![CRYSTAL ®]

Application Note

DRX™ TECHNOLOGY : A CIRRUS LOGIC DEVELOPMENT TO ENHANCE DIGITAL IMAGES

INTRODUCTION

Over the last fourteen years, Cirrus Logic, through its Crystal® product line, has developed revolutionary solutions to many difficult mixed signal problems. Our latest development efforts have resulted in a low cost and low power approach to improving the dynamic range of digital images. This short whitepaper is intended to give background information on DRX™ technology.

This new and patented approach to image data acquisition and processing makes a visible improvement in image quality. The technology is being incorporated into a family of products aimed at the entire digital camera electronics solution. Our initial product in this family is a highly integrated CCD Analog Front End. Enabled with DRX technology, these advanced products set a new standard in digital camera image qualityDRX.

DRX™

What is DRX and how does it work? These are the questions that this paper will address. First of all, let us begin with the acronym DRX. DRX stands for Dynamic Range eXtension. The purpose of DRX is to use the ADC more efficiently to get a higher dynamic range. Higher dynamic range allows you to take good pictures in bad lighting conditions such as backlighting or high contrast scenes.

DRX is composed of three blocks: the Variable Gain Amplifier or VGA, the Analog-to-digital converter or ADC and the Digital Gain Adjust block (CDS is not part of DRX and is performed ahead of DRX). The block diagram below shows the flow of data going through DRX.

DRX look at each individual pixel and amplifies it such that the maximum ADC resolution is used all the time. To better understand the process, lets look at each individual block.
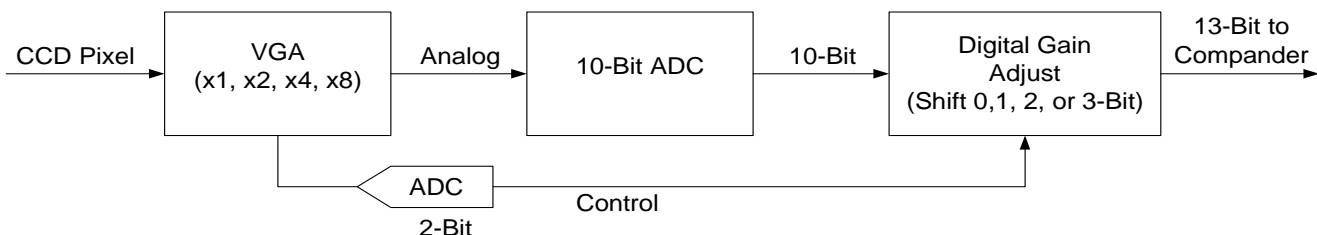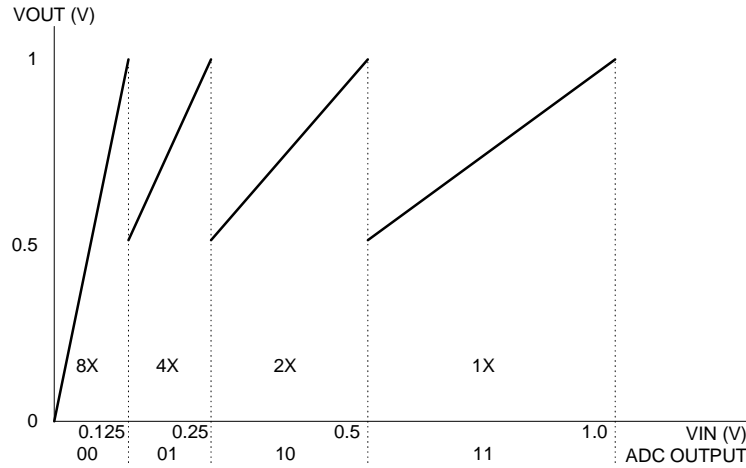

Figure 1. DRX Block Diagram

1. The VGA:

The VGA section provides a gain of x1, x2, x4 or x8 based on the input voltage (or pixel amplitude) coming from the CCD. Each pixel will be individually gained to insure a maximum use of the ADC range. The following graphics called transfer function of VGA circuit shows the curve gain, which is applied, to the input signal:

Figure 2. VGA Gain

As can seen, a lower input voltage will result in a higher analog gain. This will allows for the highest resolution possible out of the ADC until the full range of the ADC is reached. At that point, the analog gain is lowered to prevent the ADC from saturating. The analog gain applied will be accounted for in the digital section after the Analog-to-digital conversion is performed. For instance, if the analog input is 0.1V, a gain of x8 can be applied without exceeding the maximum input amplitude. Therefore the conversion will be done on 0.8V instead of 0.1V Note that the CCD RMS noise also increase with the CCD signal amplitude. . Thus the VGA provides the highest gain when the CCD noise is at its minimum.

A separate 2-bit ADC generates the corresponding digital gain control bits, theses bits are used internally to set the proper digital gain for each pixel. The extended dynamic range of the CS7620/22 can be turned off via register setting (see datasheets for details).

Example of how the VGA works:

|	**Analog Input**	**VGA gain**	**VGA control bits**	**VGA output**	**ADC input**
pixel	0.1V	x8	00	0.8V	0.8V

2. The ADC:

The ADC digitizes the input and outputs a 10-bit digital signal. The ADC does not care if the VGA is on or off. To better understand where the extended dynamic range comes from, we need to do some calculation:

For example if we have a 1.0V full-scale signal and we have a 10-bit ADC we have:
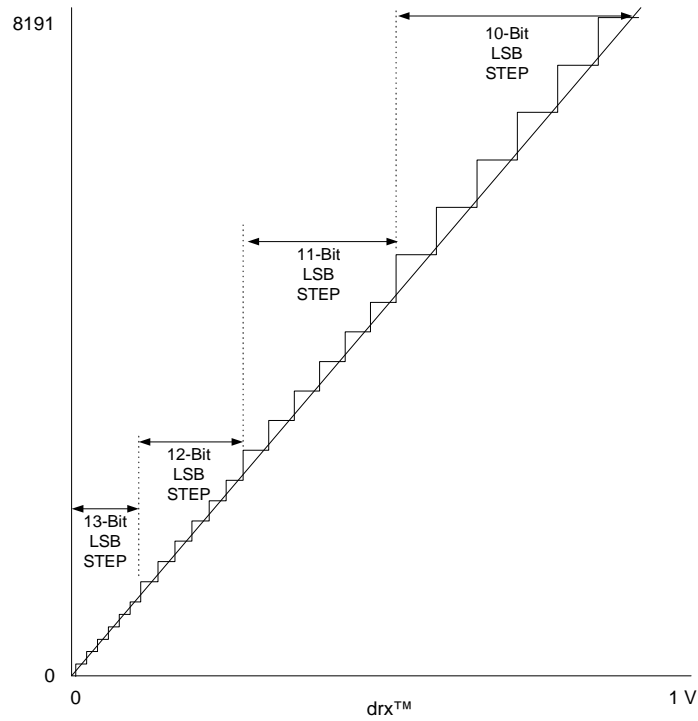
$1.0V / 2^{10} = 0.00097656$ This is your LSB step for 10-bit ADC
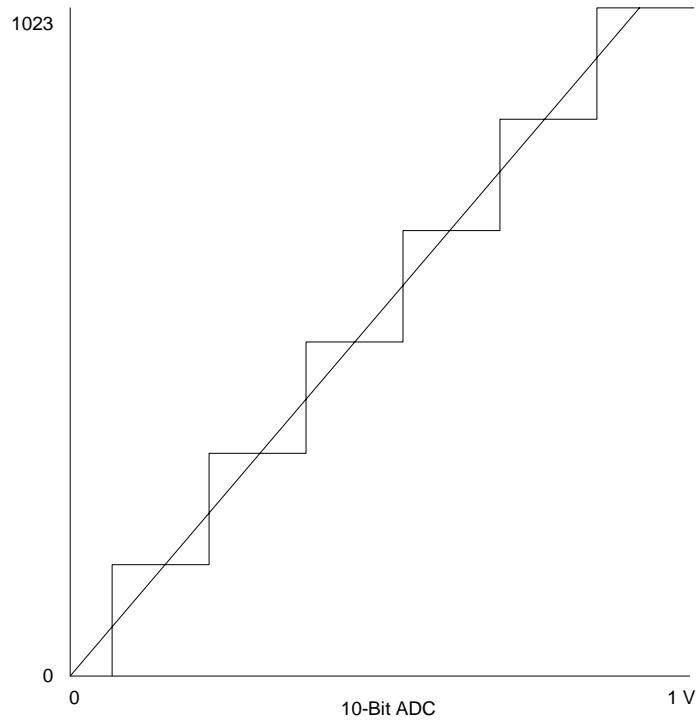
Figure 3. Quanization Step of 10 Bit ADC
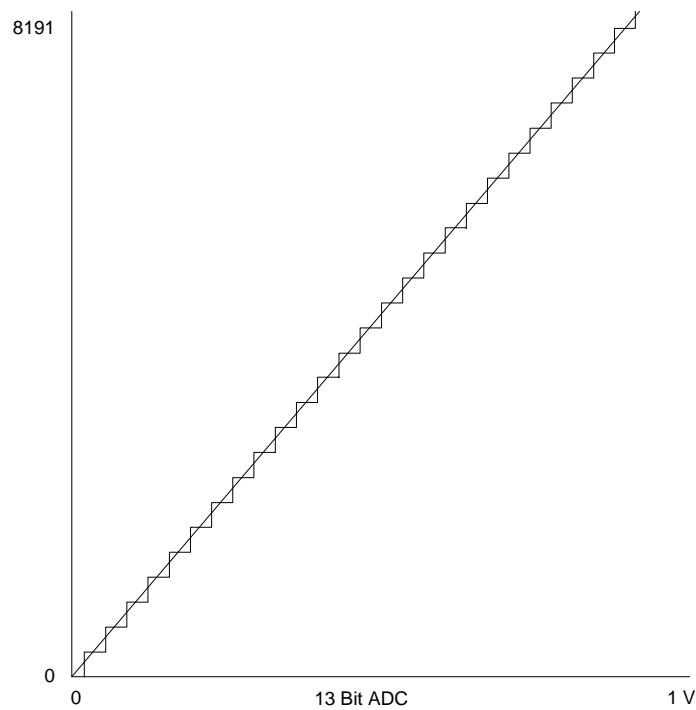
Figure 4. Quantization Step of 13 Bit ADC

Figure 5. Quantization Steps Using DRX

In our example, with the DRX technology, any signal that is less than 1/8th of the full scale (in this case 0.125V represents 1/8th of the full scale) will be gained by x8, therefore the LSB step becomes:

$0.125V / 2^{10} = 0.00012207$ This LSB step is equivalent to a 13-bit ADC.
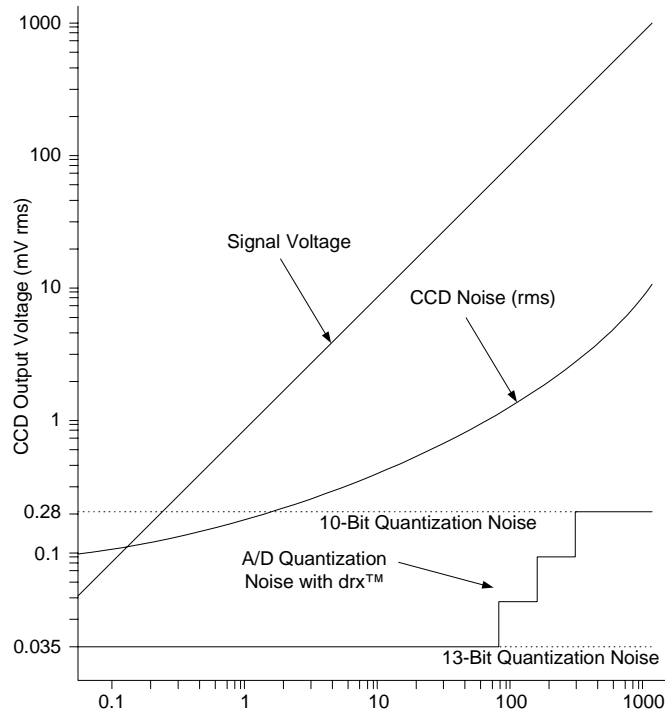
Figure 6. CCD Noise and DRX

This means that in the dark region of the image DRX will provide a better dynamic range, when it is most needed.
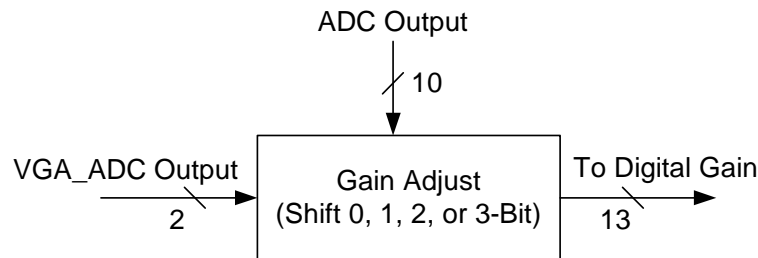
From the VGA output we have:

	ADC input	ADC output	Binary value
pixel	0.8V	1024 x (0.8V/1.0V) =819	1100110011

3. The Digital Gain Adjust:

In the Digital Gain Adjust section, the ADC output and the control bit meets to create the 13-bit output. Each digitized pixel has an individual gain associated with its 10-bit value. The Digital Gain Adjust block divides (shifts right) its output to match the analog gain performed before digitization. Note that three bits of lower significance are kept to prevent unwanted truncation.

The above explanation explains how the extended dynamic range is performed

Figure 7. Gain Adjust output Block

The three LSB are physically added in the Digital gain adjust block, in the table below the extra bits are shown in the ADC output for clarity purpose only.

From the ADC output we have:

	Binary value	VGA gain	Gain adjust output
pixel	1100110011.000	x8 -shift right 3	0001100110.011

The output of the Digital Gain Adjust is fed to the compander thus gives the full benefit of the extended dynamic range using a 10-bit output. For more details on the compander, refer to the datasheet of the CS7620 or CS7622 and AN157 CS7620/22 FAQ.

The next section addresses CCD noise and DRX technology.

Overcoming the Noise Barrier

How many bits are required in the A/D conversion of CCD data? The answer lies in the fundamental noise floor of the CCD. The A/D should not add significantly to that to maintain image quality. The noise of a CCD is due to a number of phenomena. It is composed of photon shot noise, dark-current noise, spatial noise, and thermal noise from the CCD output amplifier. The fundamental noise floor is limited by the dark-current noise at the lowest CCD output signal levels. As the CCD output signal level increases, the noise increases and is dominated by the shot noise at the low end and spatial noise at higher signal levels. This is illustrated in Figure 8.
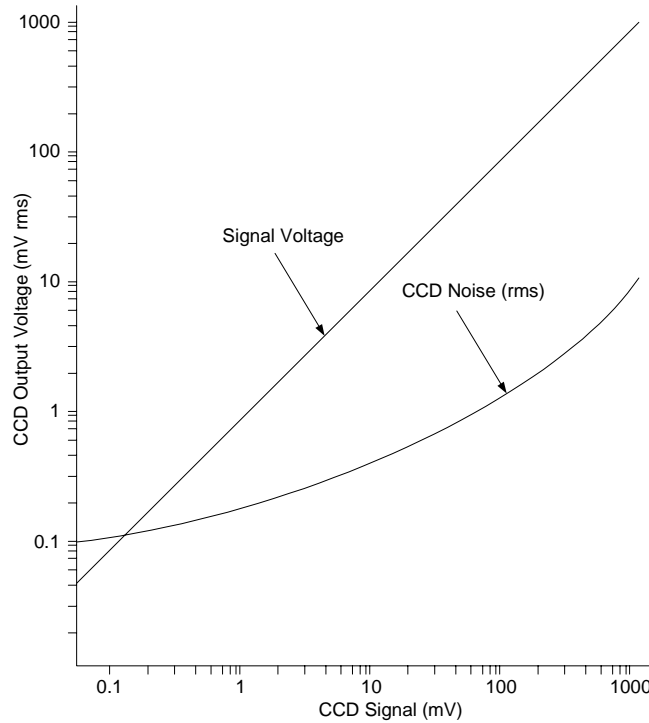
Figure 8. RMS Noise of CCD

In designing a system to capture and digitize the CCD output, the quantization noise of the system must be lower than the total noise floor illustrated in Figure 8. In addition, the A/D must accommodate the maximum output of the CCD. As illustrated in the following analysis, the noise floor of the CCD establishes the maximum value of the LSB allowed to keep quantization noise

below the CCD noise. The maximum output expected from the CCD determines the number of bits required for the A/D.

$$\text{Quantization noise} = \frac{LSB}{\sqrt{12}}$$

$$V_{\text{noise CCD}} = 100\mu V \text{ rms}$$

thus

$$LSB = 350\mu V$$

$$V_{\text{max CCD}} = 800mV$$

$$N = \frac{In\left[\frac{800mV}{350\mu V}\right]}{In(2)}$$

Therefore, a 12-bit converter is required to meet the dynamic range requirement! The resulting quantization noise using a 12-bit converter is 56 mV. Maintaining quantization noise at this level throughout the output range of the CCD is overkill. A 12-bit converter is costly in terms of power and area. A better approach is to provide a 10-bit converter at the low end where the low quantization noise is required and a lower resolution converter at the high end where CCD noise is greater and thus quantization noise can be increased. This is illustrated in Figure 6.

The way to achieve this is to have a prescaler in front of a 10-bit A/D. The prescaler supports four different gain values—high value for low signal levels and low value for high signal levels. This technique allows for increased dynamic range—13-bits in this case, while maintaining low quantization noise at the low end—without the burden of additional power and silicon area.

This new approach to image quality enhancement creates images with much better detail in both dark and light areas of the image. The attractiveness of this approach for digital cameras is that the implementation creates a marked improvement in image quality without a penalty in power consumption or processing performance.

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